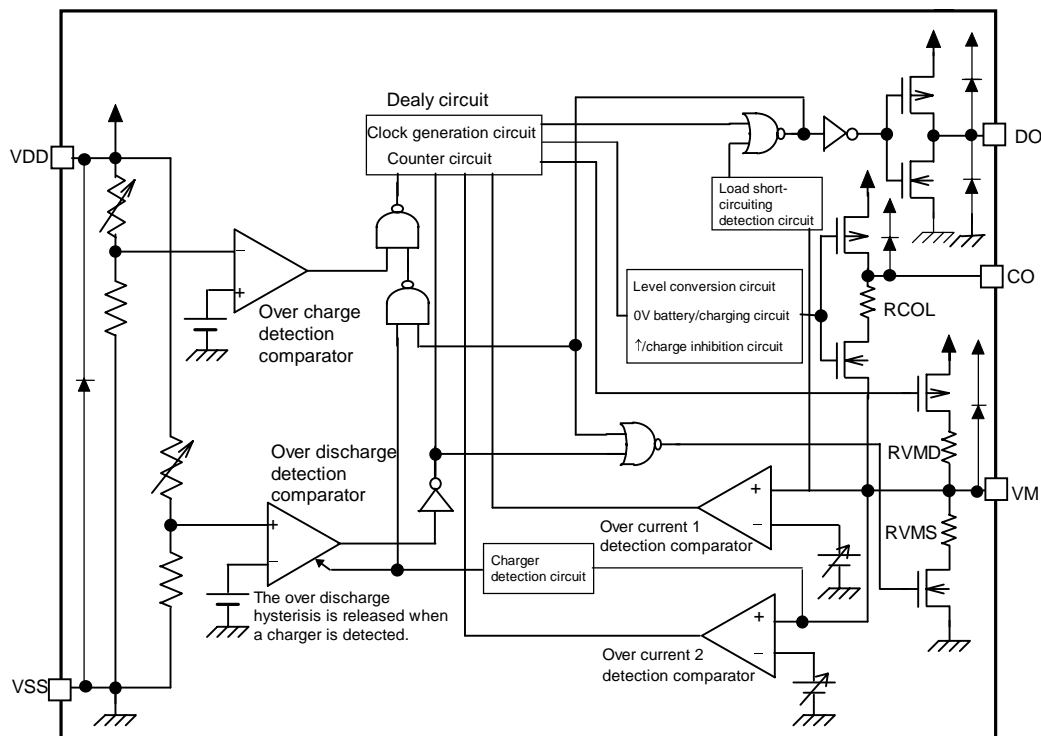


Contents

Features.....	1
Applications.....	1
Block Diagram.....	2
Selection Guide.....	2
Pin Assignment	3
Absolute Maximum Ratings.....	3
Electrical Characteristics	4
Measurement Circuits	5
Description of Operation	7
Operation Timing Chart.....	12
Battery Protection IC Connection Example	14
Precautions	15
Characteristic (typical characteristic).....	16
Dimensions, Taping	19

■ Block Diagram



Note: The diode in the IC is a parasitic diode.

Figure 1 Block Diagram

■ Selection Guide

Model No./Item	Over charge detection voltage	Over charge release voltage	Over discharge detection voltage	Over discharge release voltage	Over current 1 detection voltage	0V battery charging function
S-8241AAAMC-GAA-T2	4.275 V	4.175 V	2.3 V	2.4 V	0.100 V	available
S-8241AACMC-GAC-T2	4.350 V	4.150 V	2.3 V	3.0 V	0.100 V	available
S-8241AAOMC-GAO-T2	4.295 V	4.095 V	2.3 V	3.0 V	0.200 V	unavailable
S-8241AAPMC-GAP-T2	4.280 V	4.080 V	2.3 V	2.9 V	0.100 V	unavailable
S-8241AAQMC-GAQ-T2	4.325 V	4.075 V	2.5 V	2.9 V	0.100 V	unavailable
S-8241AARMC-GAR-T2	4.200 V	4.100 V	2.3 V	3.0 V	0.100 V	unavailable
S-8241AASMC-GAS-T2	4.325 V	4.125 V	2.3 V	2.3 V	0.100 V	available

For any changes to the detection voltage or other parameters, contact Sales Representative at SII Sales Department.

■ Pin Assignment

For details of package, refer to the attached drawing.

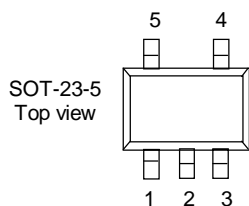


Figure 2

Pin No.	Symbol	Description
1	VM	Voltage detection pin between VM and VSS (Over current detection pin)
2	VDD	Positive power input pin
3	VSS	Negative power input pin
4	DO	FET gate connection pin for discharge control (CMOS output)
5	CO	FET gate connection pin for charge control (CMOS output)

■ Absolute Maximum Ratings

(Ta = 25°C unless otherwise specified)

Item	Symbol	Applicable pin	Rating	Unit
Input voltage between VDD and VSS *	V_{DS}	VDD	$V_{SS} - 0.3$ to $V_{SS} + 12$	V
VM Input pin voltage	V_{VM}	VM	$V_{DD} - 26$ to $V_{DD} + 0.3$	V
CO output pin voltage	V_{CO}	CO	$V_M - 0.3$ to $V_{DD} + 0.3$	V
DO output pin voltage	V_{DO}	DO	$V_{SS} - 0.3$ to $V_{DD} + 0.3$	V
Power dissipation	P_D		250	mW
Operating temperature range	Topr		-40 to +85	°C
Storage temperature range	Tstg		-40 to +125	°C

Note: This IC contains a circuit that protects it from static discharge, but take special care that no excessive static electricity or voltage which exceeds the limit of the protection circuit is applied to the IC.

* Pulse (μ sec) noise exceeding the above input voltage ($V_{SS} + 12$ V) may cause damage to the IC.

■ Electrical Characteristics

(Ta = 25°C unless otherwise specified)

Item	Symbol	Measurement conditions	Remarks	Min.	Typ.	Max.	Unit	Measurement circuit
DETECTION VOLTAGE								
Overcharge detection voltage VCU=3.9 to 4.4 V 5mV Step	VCU	1	-	VCU -0.025	VCU	VCU +0.025	V	1
			Ta= -5°C to 55°C(*1)	VCU -0.030	VCU	VCU +0.030		
Overcharge release voltage VCL-VCL=0 to 0.4 V 50mV Step	VCL	1	-	VCL -0.050	VCL	VCL +0.050	V	1
Over discharge detection voltage VDL=2.0 to 3.0 V 0.1V Step	VDL	1	-	VDL -0.080	VDL	VDL +0.080	V	1
Over discharge release voltage VDU-VDL=0 to 0.7 V 0.1V Step	VCU	1	-	VDU -0.100	VDU	VDU +0.100	V	1
Over current 1 detection voltage VIOV1=0.05 to 0.3V 5mV Step	VIOV1	2	-	VIOV1 -0.030	VIOV1	VIOV1 +0.030	V	1
Over current 2 detection voltage	VIOV2	2	-	0.4	0.5	0.6	V	1
Load short-circuiting detection voltage	VSHORT	2	VM voltage based on VDD	-1.7	-1.3	-0.6	V	1
Charger detection voltage	VCHA	3	-	-2.0	-1.3	-0.6	V	1
Over charge detection voltage temperature factor(*1)	TCOE1	-	Ta= -5°C to 55°C	-0.5	0	0.5	mV/°C	-
Over current 1 detection voltage temperature factor(*1)	TCOE2	-	Ta= -5°C to 55°C	-0.1	0	0.1	mV/°C	-
DELAY TIME								
Overcharge detection delay time	tCU	8	-	0.5	1.0	2.0	s	1
Over discharge detection delay time	tDL	8	-	62.5	125	250	ms	1
Over current 1 detection delay time	tIOV1	9	-	4	8	16	ms	1
Over current 2 detection delay time	tIOV2	9	-	1	2	4	ms	1
Load short-circuiting detection delay time	tSHORT	9	-	-	10	50	μs	1
INPUT VOLTAGE, OPERATING VOLTAGE								
Input voltage between VDD and VSS	VDS1	-	absolute maximum rating	-0.3	-	12	V	-
Input voltage between VDD and VM	VDS2	-	absolute maximum rating	-0.3	-	26	V	-
Operating voltage between VDD and VSS	VDSOP1	-	Internal circuit operating voltage	1.5	-	8	V	-
Operating voltage between VDD and VM	VDSOP2	-	Internal circuit operating voltage	1.5	-	24	V	-
CURRENT CONSUMPTION								
Current consumption during normal operation	I OPE	4	VDD=3.5V, VM=0V	1.0	3.0	6.0	μA	1
Current consumption at power down	I PDN	4	VDD=VM=1.5V	-	-	0.1	μA	1
OUTPUT RESISTANCE								
CO pin H resistance	RCOH	6	CO=3.0V, VDD=3.5V, VM=0V	0.1	2	10	kΩ	1
CO pin L resistance	RCOL	6	CO=0.5V, VDD=4.5V, VM=0V	150	600	2400	kΩ	1
DO pin H resistance	RDOH	7	DO=3.0V, VDD=3.5V, VM=0V	0.1	1.3	6.0	kΩ	1
DO pin L resistance	RDOL	7	DO=0.5V, VDD=VM=1.8V	0.1	0.5	2.0	kΩ	1
VM INTERNAL RESISTANCE								
Internal resistance between VM and VDD	RVMD	5	VDD=1.8V, VM=0V	100	300	900	kΩ	1
Internal resistance between VM and VSS	RVMS	5	VDD=VM=3.5V	35	100	200	kΩ	1
0V BATTERY CHARGING FUNCTION The 0 V battery function is either "0 V battery charging function" or "0 V battery charge inhibiting function" depending upon the product type.								
0V battery charge starting charger voltage	VOCHA	10	0V batt. cha. Available	0.0	0.8	1.5	V	1
0V battery charge inhibiting battery voltage	VOINH	11	0V batt. cha. Unavailable	0.6	0.9	1.2	V	1

(*1) : Since products are not screened by high and low temperatures, the specification for this temperature range is guaranteed by design, not production tested.

■ Measurement Circuits

Unless otherwise specified, the output voltage levels "H" and "L" at CO and DO pins are judged by the threshold voltage (1.0 V) of a Nch FET. Judge the CO pin level with respect to VM and the DO pin level with respect to VSS.

(1) Measurement Condition 1, Measurement Circuit 1

《 Over charge detection voltage, Over charge release voltage, Over discharge detection voltage, Over discharge release voltage 》

Set $V1=3.5V$ and $V2=0V$ under normal condition. Increase $V1$ from 3.5 V gradually. The voltage between VDD and VSS when $CO='L'$ is the over charge detection voltage (VCU).

Decrease $V1$ gradually. The voltage between VDD and VSS when $CO='H'$ is the over charge release voltage (VCL). Further decrease $V1$ gradually. The voltage between VDD and VSS when $DO='L'$ is the over discharge detection voltage (VDL). Increase $V1$ gradually. The voltage between VDD and VSS when $DO='H'$ is the over discharge release voltage (VDU).

(2) Measurement Condition 2, Measurement Circuit 1

《 Over current 1 detection voltage, Over current 1 release voltage, Over current 2 detection voltage, Load short-circuiting detection voltage 》

Set $V1=3.5V$ and $V2=0V$ under normal condition. Increase $V2$ from 0 V gradually. The voltage between VM and VSS when $DO='L'$ is the over current 1 detection voltage (VIOV1).

Set $V1=3.5V$ and $V2=0V$ under normal condition. Increase $V2$ from 0 V at a rate of 1 ms to 4 ms. The voltage between VM and VSS when $DO='L'$ is the over current 2 detection voltage (VIOV2).

Set $V1=3.5V$ and $V2=0V$ under normal condition. Increase $V2$ from 0 V at a rate of 1 μs to 50 μs . The voltage between VM and VDD when $DO='L'$ is the load short-circuiting detection voltage (VSHORT).

(3) Measurement Condition 3, Measurement Circuit 1

《 Charger detection voltage, (=abnormal charge current detection voltage) 》

Set $V1=1.8V$ and $V2=0V$ under over discharge condition. Increase $V1$ gradually, set $V1=(VDU+VDL)/2$ (within over discharge hysteresis, over discharge condition), then decrease $V2$ from 0 V gradually. The voltage between VM and VSS when $DO='H'$ is the charger detection voltage (VCHA).

Set $V1=3.5V$ and $V2=0V$ under normal condition. Decrease $V2$ from 0 V gradually. The voltage between VM and VSS when $CO='L'$ is the abnormal charge current detection voltage.

The abnormal charge current detection voltage has the same value as the charger detection voltage.

(4) Measurement Condition 4, Measurement Circuit 1

《 Normal operation consumption current, Power-down consumption current 》

Set $V1=3.5V$ and $V2=0V$ under normal condition. The current I_{DD} flowing through VDD pin is the normal operation consumption current (IOPE).

Set $V1=V2=1.5V$ under over discharge condition. The current I_{DD} flowing through VDD pin is the power-down consumption current (IPDN).

(5) Measurement Condition 5, Measurement Circuit 1

⟨⟨ Internal resistance between VM and VDD, Internal resistance between VM and VSS ⟩⟩

Set $V1=1.8V$ and $V2=0V$ under over discharge condition. Measure current I_{VM} flowing through VM pin. $1.8V/|I_{VM}|$ is the internal resistance (R_{VMD}) between VM and VDD.

Set $V1=V2=3.5V$ under over current condition. Measure current I_{VM} flowing through VM pin. $3.5V/|I_{VM}|$ is the internal resistance (R_{VMS}) between VM and VSS.

(6) Measurement Condition 6, Measurement Circuit 1

⟨⟨ CO pin H resistance, CO pin L resistance ⟩⟩

Set $V1=3.5V$, $V2=0V$ and $V3=3.0V$ under normal condition. Measure current I_{CO} flowing through CO pin. $0.5V/|I_{CO}|$ is the CO pin H resistance (R_{COH}).

Set $V1=4.5V$, $V2=0V$ and $V3=0.5V$ under over charge condition. Measure current I_{CO} flowing through CO pin. $0.5V/|I_{CO}|$ is the CO pin L resistance (R_{COL}).

(7) Measurement Condition 7, Measurement Circuit 1

⟨⟨ DO pin H resistance, DO pin L resistance ⟩⟩

Set $V1=3.5V$, $V2=0V$ and $V4=3.0V$ under normal condition. Measure current I_{DO} flowing through DO pin. $0.5V/|I_{DO}|$ is the DO pin H resistance (R_{DOH}).

Set $V1=1.8V$, $V2=0V$ and $V4=0.5V$ under over discharge condition. Measure current I_{DO} flowing through DO pin. $0.5V/|I_{DO}|$ is the DO pin L resistance (R_{DOL}).

(8) Measurement Condition 8, Measurement Circuit 1

⟨⟨ Over charge detection delay time, Over discharge detection delay time ⟩⟩

Set $V1=3.5V$ and $V2=0V$ under normal condition. Increase $V1$ gradually to over charge detection voltage (V_{CU}) - 0.2 V and increase $V1$ to the over charge detection voltage (V_{CU}) + 0.2 V momentarily (within 10 μ s). The time after $V1$ becomes the over charge detection voltage until CO goes "L" is the over charge detection delay time (t_{CU}).

Set $V1=3.5V$ and $V2=0V$ under normal condition. Decrease $V1$ gradually to over discharge detection voltage (V_{DL}) + 0.2 V and decrease $V1$ to the over discharge detection voltage (V_{DL}) - 0.2 V momentarily (within 10 μ s). The time after $V1$ becomes the over discharge detection voltage (V_{DL}) until DO goes "L" is the over discharge detection delay time (t_{DL}).

(9) Measurement Condition 9, Measurement Circuit 1

⟨⟨ Over current 1 detection delay time, Over current 2 detection delay time, Load short-circuiting detection delay time, Abnormal charge current detection delay time ⟩⟩

Set $V1=3.5V$ and $V2=0V$ under normal condition. Increase $V2$ from 0 V to 0.35 V momentarily (within 10 μ s). The time after $V2$ becomes over current 1 detection voltage (V_{IOV1}) until DO goes "L" is over current 1 detection delay time (t_{IOV1}).

Set $V1=3.5V$ and $V2=0V$ under normal condition. Increase $V2$ from 0 V to 0.7 V momentarily (within 1 μ s). The time after $V2$ becomes over current 1 detection voltage (V_{IOV1}) until DO goes "L" is over current 2 detection delay time (t_{IOV2}).

Note!) Over current 2 detection delay time begins when over current 1 is detected. (Because the delay circuit is shared.)

Set $V1=3.5V$ and $V2=0V$ under normal condition. Increase $V2$ from 0 V to 3.0 V momentarily (within 1 μ s). The time after $V2$ becomes the load short-circuiting detection voltage (V_{SHORT}) until DO goes "L" is the load short-circuiting detection delay time (t_{SHORT}).

Set $V1=3.5V$ and $V2=0V$ under normal condition. Decrease $V2$ from 0 V to -2.5 V momentarily

(within 10 μ s). The time after V2 becomes the charger detection voltage (VCHA) until CO goes "L" is the abnormal charge current detection delay time.

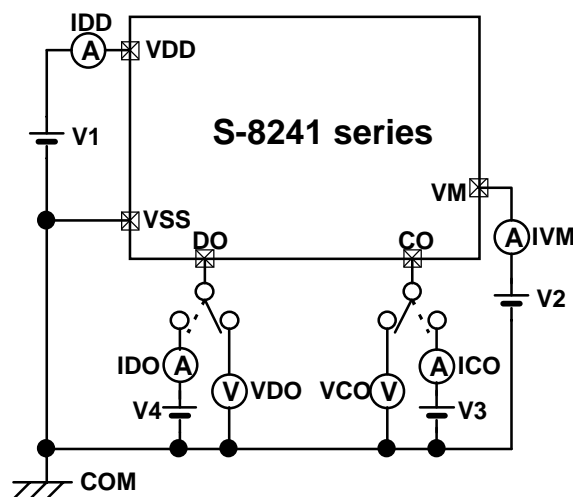
The abnormal charge current detection delay time has the same value as the over charge detection delay time.

- (10) Measurement Condition 10, Measurement Circuit 1 (Product with 0V battery charging function)
 << 0V battery charge start charger voltage >>

Set V1=V2=0V and decrease V2 gradually. The voltage between VDD and VM when CO='H' (VM + 0.1 V or higher) is the 0V battery charge start charger voltage (V0CHA).

- (11) Measurement Condition 11, Measurement Circuit 1 (Product with 0V battery charge inhibiting function)
 << 0V battery charge inhibiting battery voltage >>

Set V1=0V and V2=4V. Increase V1 gradually. The voltage between VDD and VSS when CO='H' (VM + 0.1 V or higher) is the 0V battery charge inhibiting battery voltage (V0INH).



Measurement circuit 1

Figure 3

■ Description of Operation

Normal condition

This IC monitors the voltage of the battery connected to VDD and VSS pins and the differences in voltages between VM and VSS pins to control charging and discharging. If the battery voltage is in the range from the over discharge detection voltage (VDL) to the over charge detection voltage (VCU), and the VM pin voltage is in the range from the charger detection voltage (VCHA) to the over current 1 detection voltage (VIOV1) (the current flowing through the battery is equal to or lower than a specified value), both the charging and discharging control FETs turn on. In this condition, charging and discharging can be carried out freely. This condition is called the normal condition.

Over current condition

If the discharging current becomes equal to or higher than a specified value (the VM pin voltage is equal to or higher than the over current detection voltage) during discharging under normal condition and it continues for the over current detection delay time or longer, the discharging control FET turns off to stop discharging. This condition is called an over current condition. (The over current means

over current 1, over current 2, or load short-circuiting.)

The VM and VSS pins are shorted by the RVMS resistor in the IC under the over current condition.

When a load is connected, the VM pin voltage equals the VDD potential due to the load.

The over current condition returns to the normal condition when the load is released and the impedance between the EB+ and EB- pins (see Figure 9 for a connection example) is the automatic recoverable load resistance (see the equation [1] below) or higher. When the load is removed, the VM pin, which and the VSS pin are shorted with the RVMS resistor, goes back to the VSS potential. The IC detects that the VM pin potential returns to over current 1 detection voltage (VIOV1) or lower and returns to the normal condition.

Automatic recoverable load resistance = {Battery voltage / (Minimum value of over current 1 detection voltage) - 1} x (RVMS maximum value) --- [1]

Example: Battery voltage = 3.5 V and over current 1 detection voltage (VIOV1) = 0.1 V

Automatic recoverable load resistance = (3.5 V / 0.07 V - 1) x 200kΩ = 9.8MΩ

*Note: The automatic recoverable load resistance is different with the battery voltage and over current 1 detection voltage settings.
To enable automatic recovery from over current, check the over current 1 detection voltage setting for the IC to be used, and determine the minimum value of the open load using the above equation [1].

Over charge condition

If the battery voltage becomes higher than the over charge detection voltage (VCU) during charging under normal condition and it continues for the over charge detection delay time (tCU) or longer, the charging control FET turns off to stop charging. This condition is called an over charge condition.

The over charge condition is released in two cases (① and ②) for each of the products with and without over charge hysteresis:

- ◆ Products with over charge hysteresis (Over charge detection voltage (VCU) > Over charge release voltage (VCL))
 - ① If the battery voltage falls below the over charge release voltage (VCL), the charging control FET turns on and the normal condition returns.
 - ② If a load is installed and discharging starts, the charging control FET turns on and the normal condition returns. The release mechanism is as follows: the discharge current flows through an internal parasitic diode of the charging FET immediately after a load is installed and discharging starts, and the VM pin voltage increases by about 0.7 V (Vf voltage of the diode) from the VSS pin voltage momentarily. The IC detects this voltage (over current 1 detection voltage or higher) and releases the over charge condition. Consequently, if the battery voltage is equal to or lower than the over charge detection voltage (VCU), the normal condition returns immediately. If the battery voltage is higher than the over charge detection voltage (VCU), the normal condition does not return until the battery voltage falls below the over charge detection voltage (VCU) even if a load is installed. If the VM pin voltage is equal to or lower than the over current 1 detection voltage when a load is installed and discharging starts, the normal condition does not return.

!Note:

If the battery is charged to a voltage higher than the over charge detection voltage (VCU) and the battery voltage does not fall below the over charge detection voltage (VCU) even when a heavy load (which causes an over current) is installed, detection/delay of over current 1 and over current 2 do not work until the battery voltage falls below the over charge detection voltage (VCU). However, an actual battery has an internal impedance of several dozens of mΩ, and the battery voltage drops immediately after a heavy load which causes an over current is installed, and therefore, detection/delay of over current 1 and over current 2 work. Detection/delay of load short-circuiting work regardless of the battery voltage.

- ◆ Products without over charge hysteresis (Over charge detection voltage (VCU) = Over charge release voltage (VCL))
- ① If the battery voltage falls below the over charge release voltage (VCL), the charging control FET turns on and the normal condition returns.
- ② If a load is installed and discharging starts, the charging control FET turns on and the normal condition returns. The release mechanism is as follows: the discharge current flows through an internal parasitic diode of the charging FET immediately after a load is installed and discharging starts, and the VM pin voltage increases by about 0.7 V (V_f voltage of the diode) from the VSS pin voltage momentarily. The IC detects this voltage (over current 1 detection voltage or higher), increases the over charge detection voltage by about 50 mV, and releases the over charge condition. Consequently, if the battery voltage is equal to or lower than the over charge detection voltage (VCU) + 50 mV, the normal condition returns immediately. If the battery voltage is higher than the over charge detection voltage (VCU) + 50 mV, the normal condition does not return until the battery voltage falls below the over charge detection voltage (VCU) + 50 mV even if a load is installed. If the VM pin voltage is equal to or lower than the over current 1 detection voltage when a load is installed and discharging starts, the normal condition does not return.

!Note:

If the battery is charged to a voltage higher than the over charge detection voltage (VCU) and the battery voltage does not fall below the over charge detection voltage (VCU) + 50 mV even when a heavy load (which causes an over current) is installed, detection/delay of over current 1 and over current 2 do not work until the battery voltage falls below the over charge detection voltage (VCU) + 50 mV. However, an actual battery has an internal impedance of several dozens of $m\Omega$, and the battery voltage drops immediately after a heavy load which causes an over current is installed, and therefore, detection/delay of over current 1 and over current 2 work. Detection/delay of load short-circuiting work regardless of the battery voltage.

Over discharge condition

If the battery voltage falls below the over discharge detection voltage (VDL) during discharging under normal condition and it continues for the over discharge detection delay time (tDL) or longer, the discharging control FET turns off and discharging stops. This condition is called the over discharge condition. When the discharging control FET turns off, the VM pin is pulled up by the RVMD resistor between VM and VDD in the IC. If the potential difference between VM and VDD falls below 1.3 V (typ.) (load short-circuiting detection voltage), the IC's current consumption is reduced to the power-down current consumption (IPDN). This condition is called the power-down condition. The VM and VDD pins are shorted by the RVMD resistor in the IC under the over discharge and power-down conditions.

The power-down condition is released when the charger is connected and the potential difference between VM and VDD becomes 1.3 V (typ.) or higher (load short-circuiting detection voltage). At this time, the FET is still off. When the battery voltage becomes equal to or higher than the over discharge release voltage (VDU) in this condition, the FET turns on and the over discharge condition changes to the normal condition.

Charger detection

If the VM pin voltage is lower than the charger detection voltage (VCHA) when an over-discharged battery is connected with a charger, over discharge hysteresis is released, and when the battery voltage becomes equal to or higher than the over discharge detection voltage (VDL), the discharging control FET turns on. This action is called charger detection. (The charge time can be reduced via the internal parasitic diode in the discharging control FET by using this charger detection.)

Abnormal charge current detection

If the VM pin voltage falls below the charger detection voltage (VCHA) during charging under normal condition and it continues for the over charge detection delay time (tCU) or longer, the charging control FET turns off and charging stops. This action is called abnormal charge current detection. Abnormal charge current detection works if the discharging control FET turns on (DO pin voltage is "H") and the VM pin voltage falls below the charger detection voltage (VCHA). Consequently, if an abnormal charge current flows to an over-discharged battery, the charging control FET turns off and charging stops after the battery voltage becomes the over discharge detection voltage or higher (DO pin voltage becomes "H") and the over charge detection delay time (tCU) elapses.

Abnormal charge current detection is released when the voltage difference between VM pin and VSS pin becomes less than charger detection voltage (VCHA) by separating the charger.

Since the 0V battery charging function has higher priority than the abnormal charge current detection function, abnormal charge current may not be detected while the battery voltage is low for product with the 0V battery charging function.

Delay circuits

The following delay times are generated by dividing the about 2kHz clock with a counter.

- Over charge detection delay time (= abnormal charge current detection delay time): 1.0s
- Over discharge detection delay time: 125 ms
- Over current 1 detection delay time: 8 ms
- Over current 2 detection delay time: 2 ms

Note!

- Over current 2 detection delay time starts when over current 1 is detected. Consequently, if over current 2 is detected after over current 2 detection delay time passes after over current 1 detection, the discharging control FET turns off. At this time, over current 2 detection delay time may seem to be increased (or over current 1 detection delay time may seem to be decreased.)

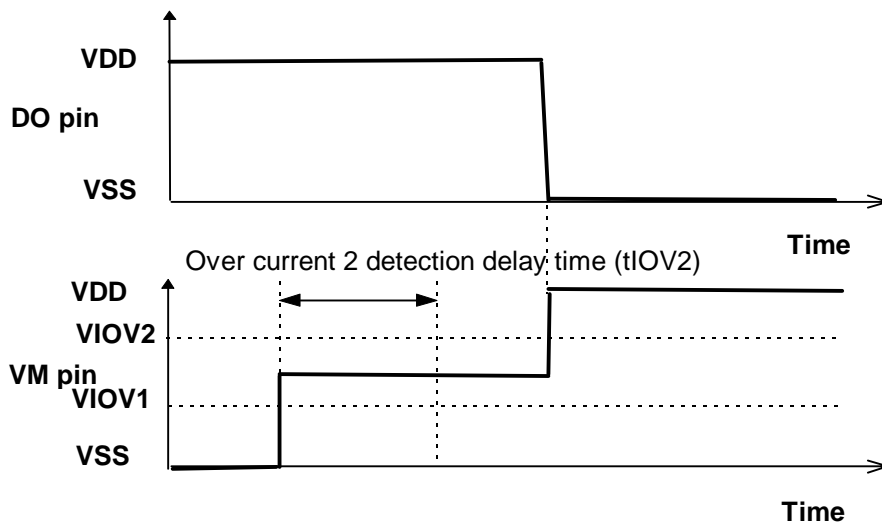


Figure 4

- If an over current condition (over current 1, over current 2 and load short-circuiting) is detected and it continues for the over discharge detection delay time or longer without releasing a load, the condition changes to the power-down condition when the battery voltage falls below the over discharge detection voltage. If the battery voltage falls below the over discharge detection voltage due to an over current, the discharging control FET turns off when the over current is detected. If the battery voltage restores late and the battery voltage after the over discharge detection delay time is equal to or lower than the over discharge detection voltage, the condition changes to the power-down condition.

0V battery charging function (*1) (*2)

This function is used to recharge the connected battery after it self-discharges to 0 V. When the 0V battery charging start charger voltage (V0CHA) or higher is applied to between EB+ and EB- pins by connecting the charger, the charging control FET gate is fixed to VDD potential. When the voltage between the gate and source of the charging control FET becomes equal to or higher than the turn-on voltage by the charger voltage, the charging control FET turns on to start charging. At this time, the discharging control FET turns off and the charging current flows through the internal parasitic diode in the discharging control FET. If the battery voltage becomes equal to or higher than the over discharge release voltage (VDU), the normal condition returns.

0V battery charge inhibiting function (*1)

This function is used to inhibit recharge the connected battery if it is short-circuited (0 V) internally. If the battery voltage becomes 0.9 V (typ.) or lower, the charging control FET gate is fixed to EB- potential to inhibit charging. If the battery voltage is the 0V battery charge inhibiting battery voltage (V0INH) or higher, charging can be performed.

- (*1) Some battery providers do not recommend charge for 0V batteries(complete self-discharged). Please refer to battery providers.
- (*2) The 0V battery charging function has higher priority than the abnormal charge current detection function. Consequently, a product with the 0V battery charging function can be charged and abnormal charge current cannot be detected when the battery voltage is low (maximum 1.8 V or lower).
- (*3) When a battery is connected to an IC for the first time, the IC may not enter the normal condition (not dischargeable condition). If this occurs, set the VM pin voltage equal to the VSS voltage (short the VM and VSS pins or connect a charger) to enter the normal condition.

■ Operation Timing Chart

1. Over charge and over discharge detection

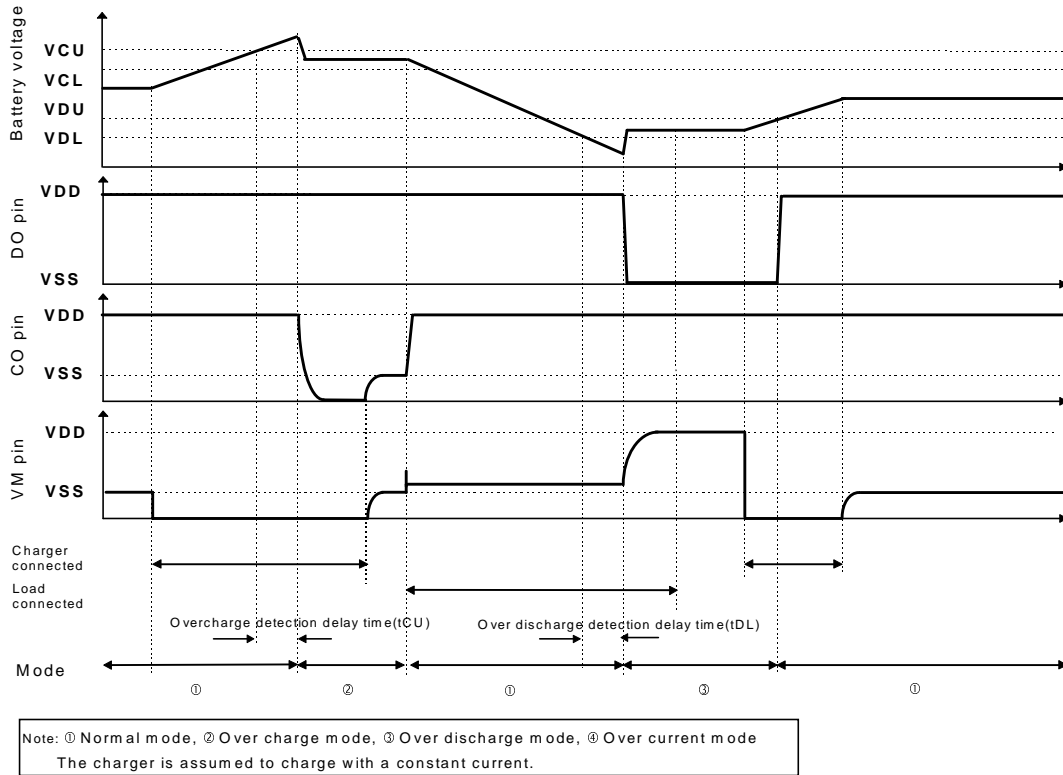


Figure 5

2. Over current detection

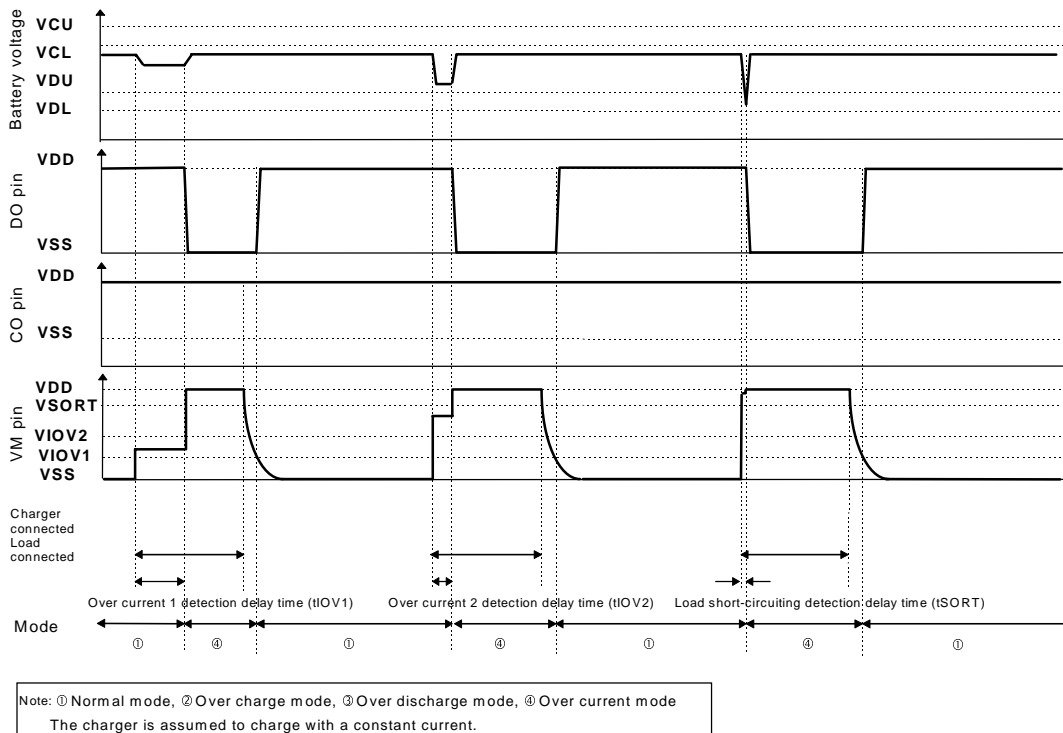


Figure 6

3. Charger detection

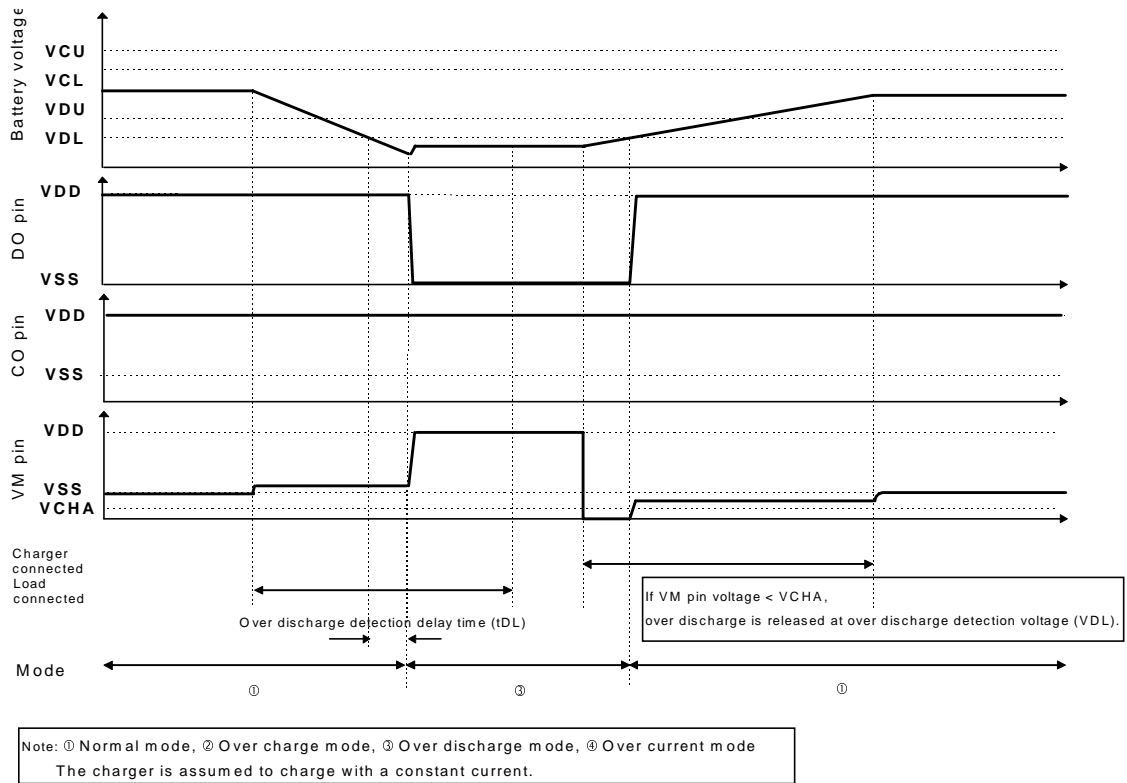


Figure 7

4. Abnormal charge current detection

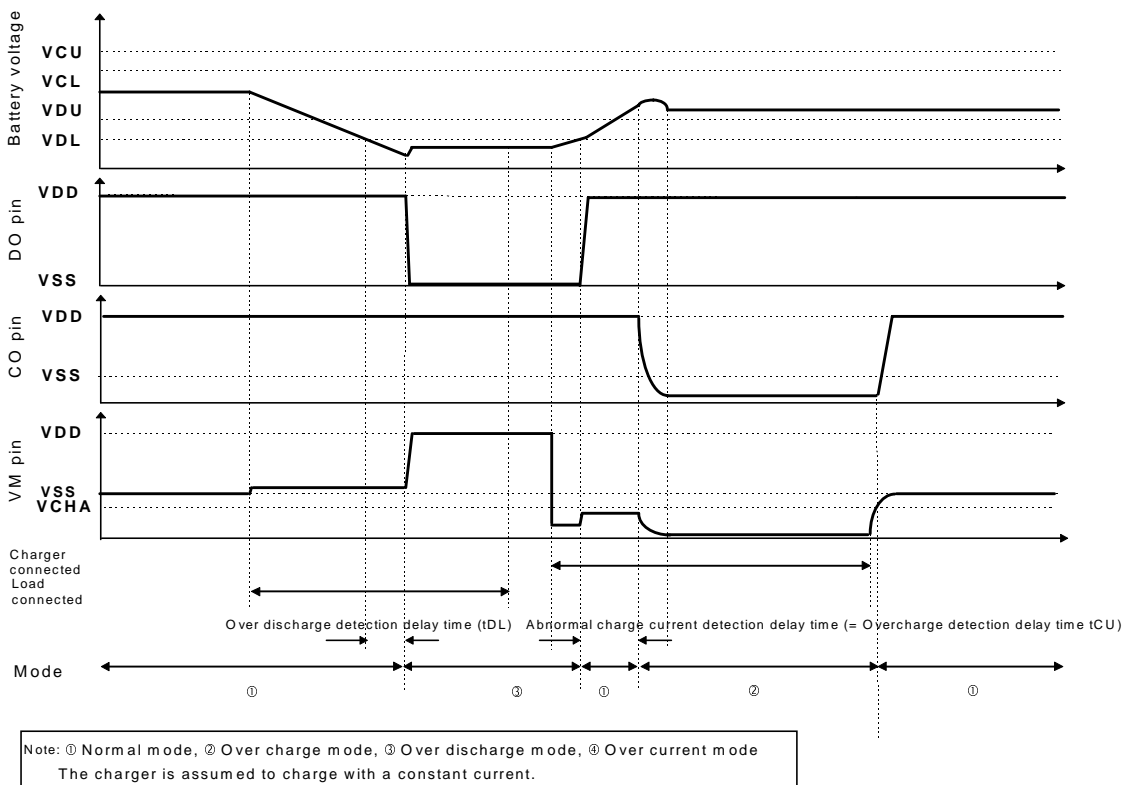


Figure 8

■ Battery Protection IC Connection Example

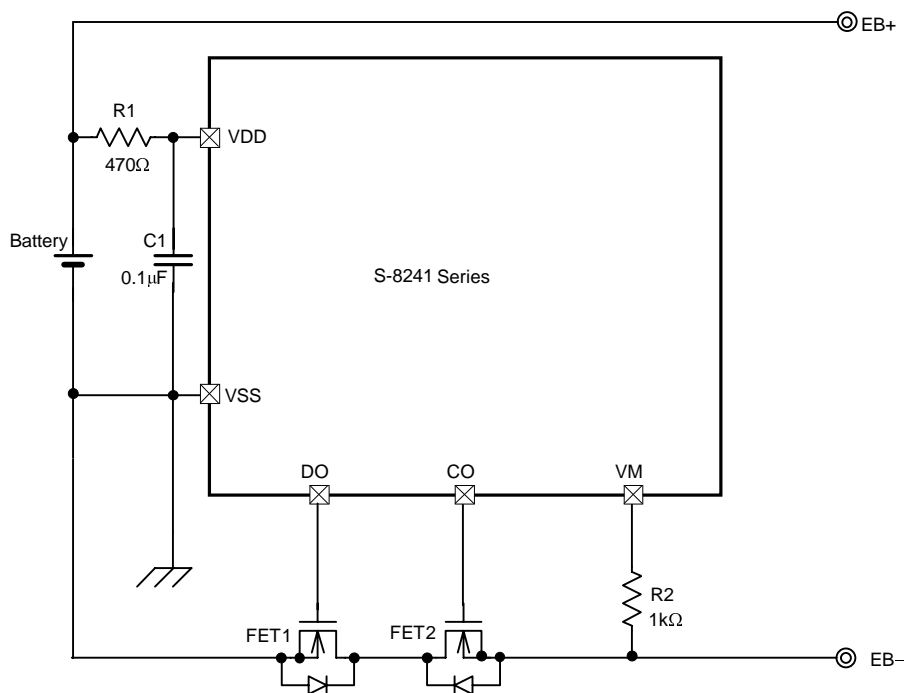


Figure 9

Table 1 Constant

Symbol	Parts	Purpose	Recommend	min.	max.	Remarks
FET1	Nch MOS_FET	Charge control	-----	-----	-----	*1) $0.4\text{ V} \leq \text{Threshold voltage} \leq$ Over discharge detection voltage Withstand voltage between gate and source \geq Charger voltage
FET2	Nch MOS_FET	Discharge control	-----	-----	-----	*1) $0.4\text{ V} \leq \text{Threshold voltage} \leq$ Over discharge detection voltage Withstand voltage between gate and source \geq Charger voltage
R1	Resistor	For ESD For power fluctuation	470Ω	300Ω	The same value as the R2	*2) Set resistance so that $R1 \leq$ R2.
C1	Capacitor	For power fluctuation	0.1μF	0.01μF	1.0 μF	*3) Install a capacitor of 0.01 μF or higher between VDD and VSS.
R2	Resistor	Protection at reverse connecting a charger	1KΩ	300Ω	1KΩ	*4) If it is less than 300Ω, discharging cannot be stopped when the charger is connected reversely.

Note: These values are based on the results of the current evaluation (as of July 9, 1999). They may be changed according to future evaluation.

- *1) If an FET with a threshold voltage of 0.4 V or lower is used, the charging current may not be able to be cut.
If an FET with a threshold voltage equal to or higher than the over discharge detection voltage is used, discharging may stop before over discharge is detected.
If the withstand voltage between the gate and source is lower than the charger voltage, the FET may be destroyed.
- *2) If R1 has a higher resistance than R2 and the charger is connected reversely, current flows from the charger to the IC, and the voltage between VDD and VSS may exceed the absolute maximum rating.
Install a resistor of 300Ω or higher as R1 for ESD protection.
If R1 has a high resistance, the over charge detection voltage increases by IC current consumption.
- *3) If a capacitor of less than 0.01 μF is installed as C1, DO may oscillate when load short-circuiting is detected, a charger is connected reversely, or over current 1 or 2 is detected.
Be sure to install a capacitor of 0.01 μF or higher as C1. With some types of batteries, DO oscillation may not stop unless the C1 capacity is increased. Set the C1 capacity by evaluating actual applications.

-
- *4) If R2 is set to less than 300 Ω , a current which is higher than the permissible loss (power dissipation) flows through the IC and it may be damaged when the charger is connected reversely. If a resistor of higher than 1k Ω is installed as R2, the charging current may not be cut when a high-voltage charger is connected.

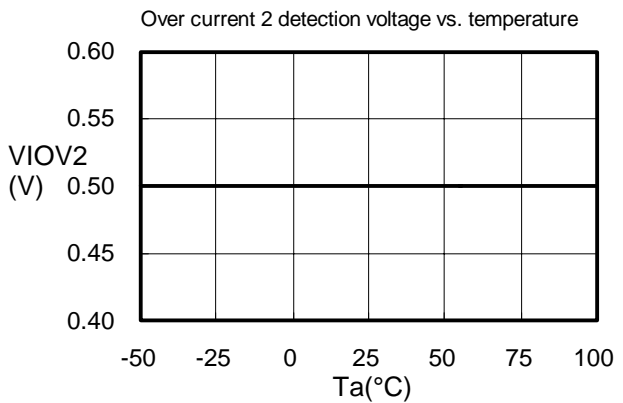
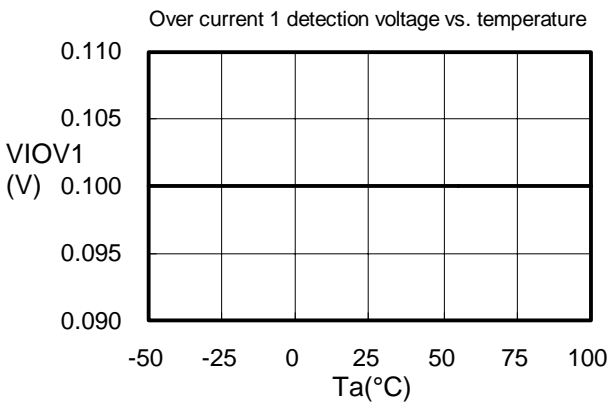
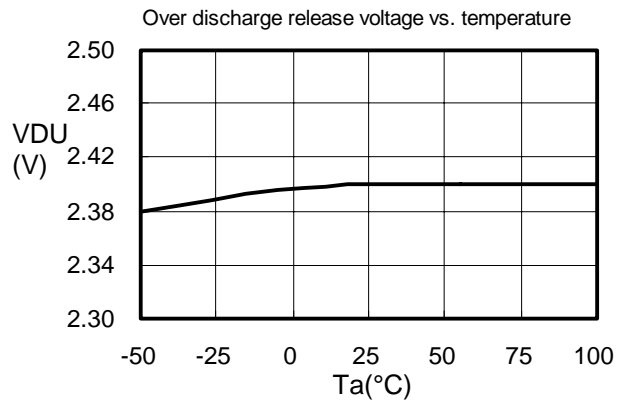
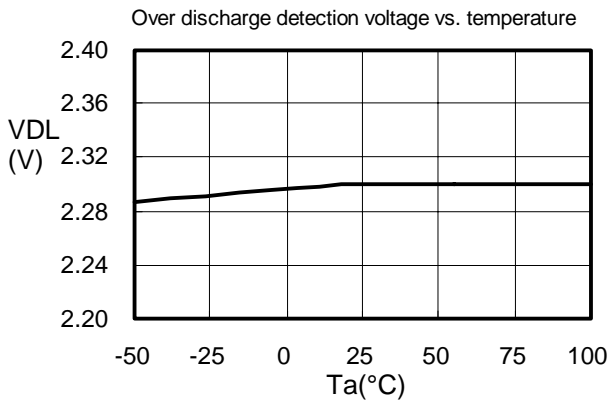
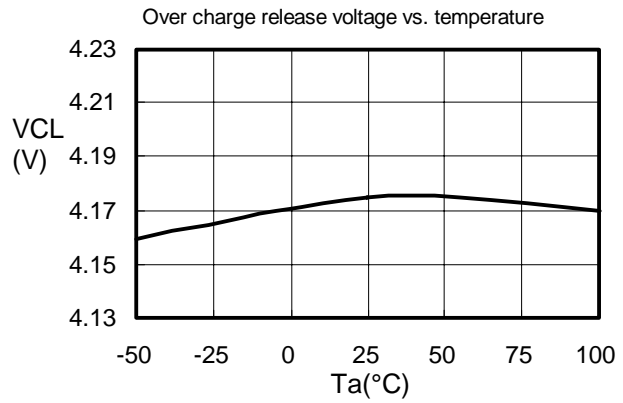
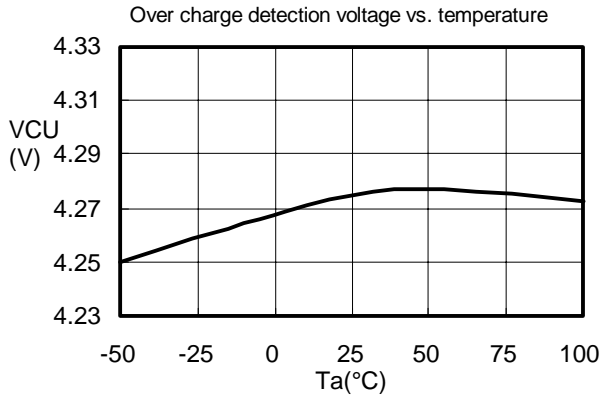
!Note: The above connection diagram and constants do not guarantee proper operations. Evaluate your actual application and set constants properly.

■ Precautions

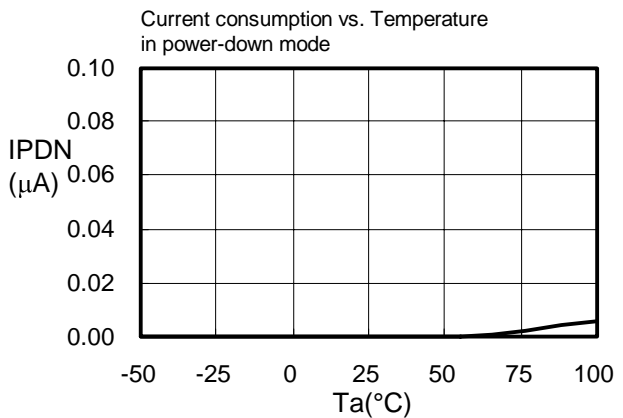
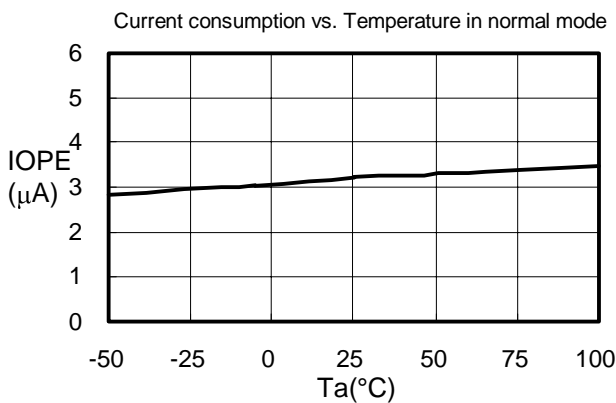
- Pay attention to the operating conditions for input/output voltage and load current so that the loss of the IC does not exceed the permissible loss (power dissipation) of the package.
- Seiko Instruments Inc. shall not be responsible for any patent infringement by products including the S-8241 Series in connection with the method of using the S-8241 Series in such products, the product specifications or the country of destination thereof.

■ Characteristic (typical characteristic)

1. Detection/release voltage temperature characteristics

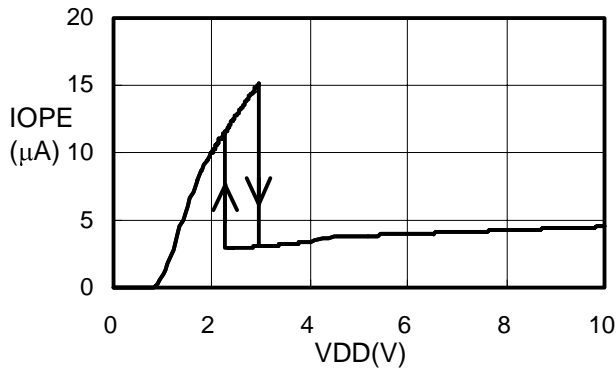


2. Current consumption temperature characteristics

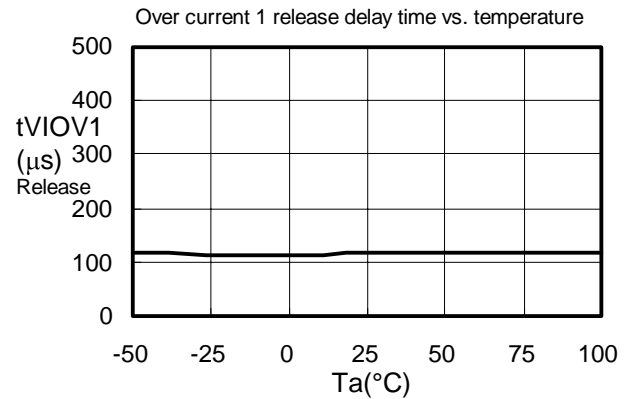
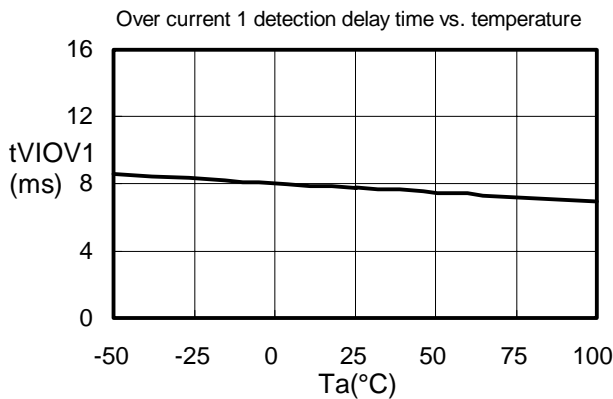
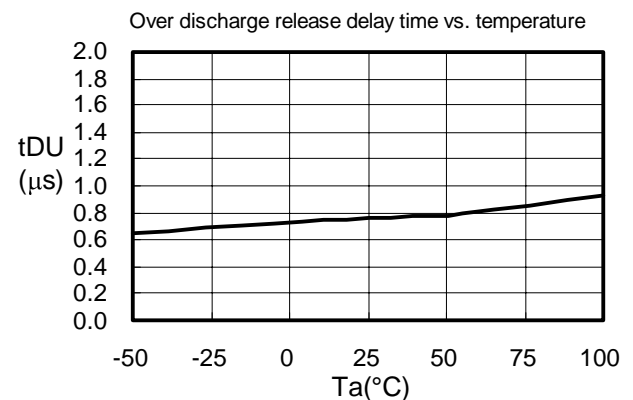
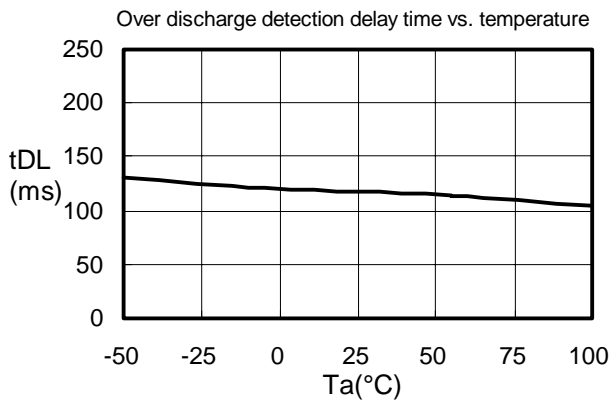
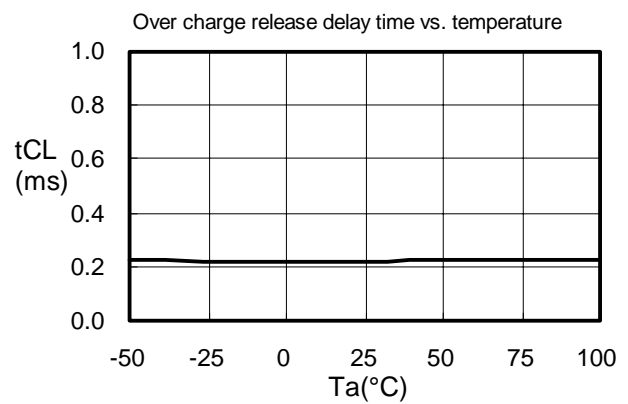
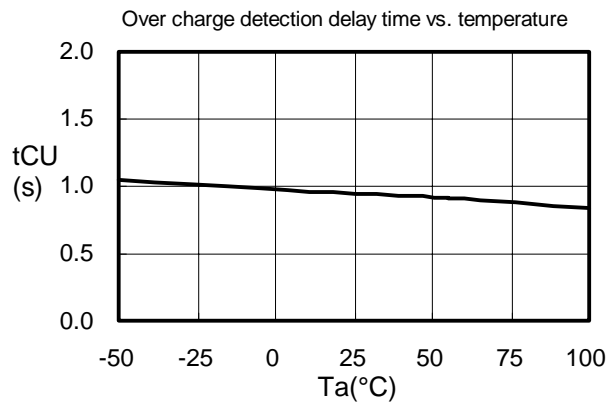


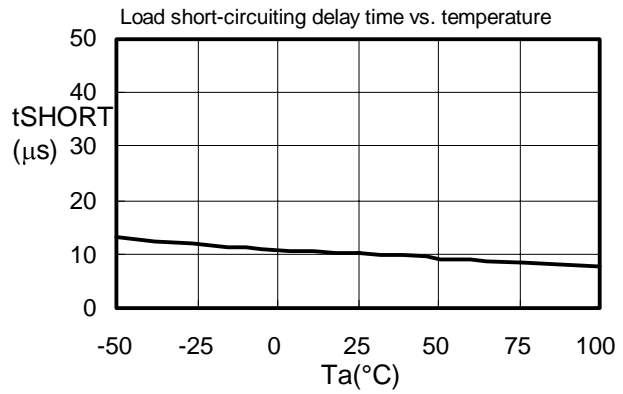
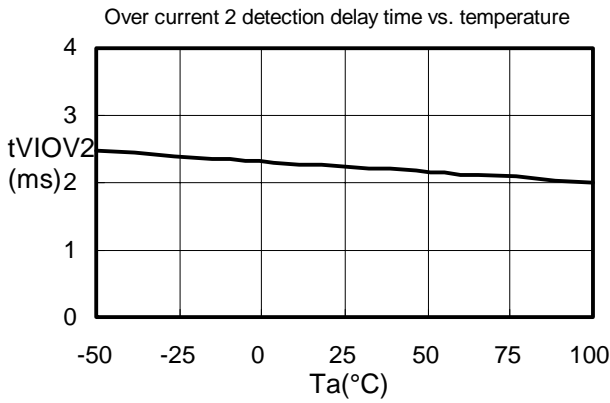
3. Current consumption Power voltage characteristics (Ta=25°C)

Current consumption - -
power supply volatge dependency VM=VSS

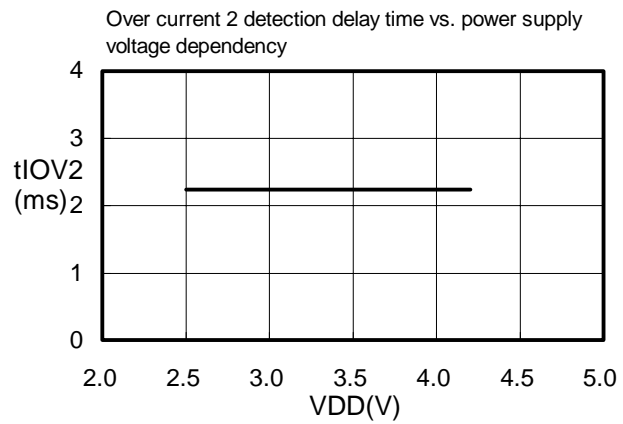
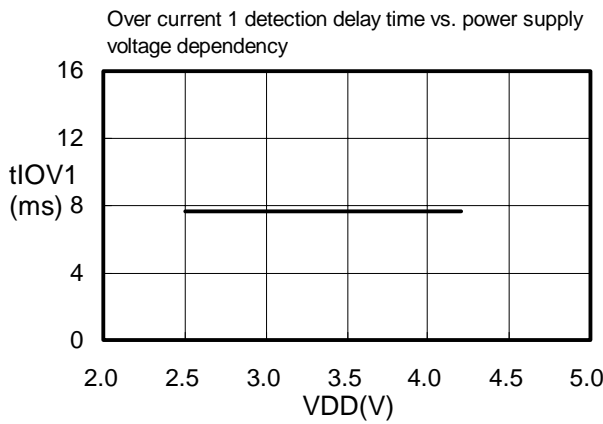


4. Detection/release delay time temperature characteristics

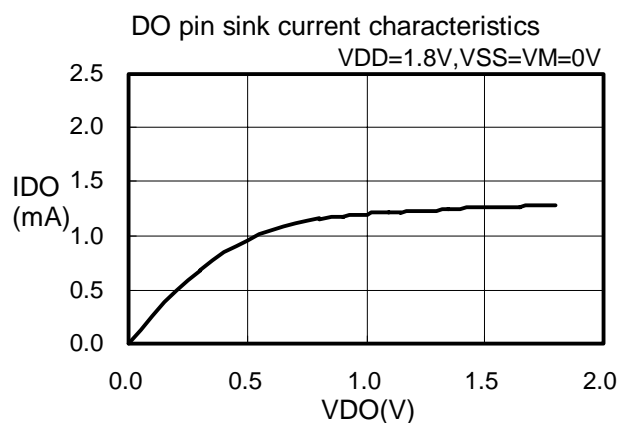
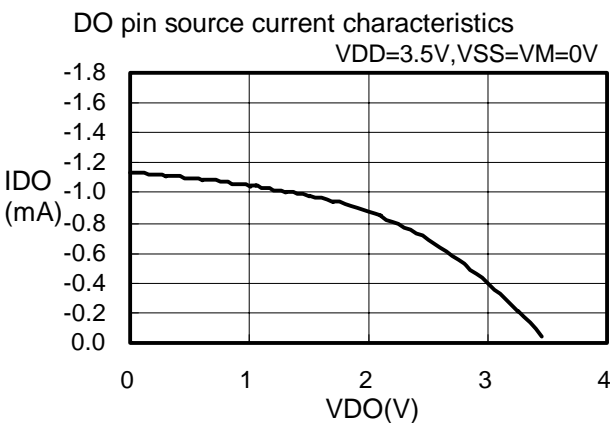
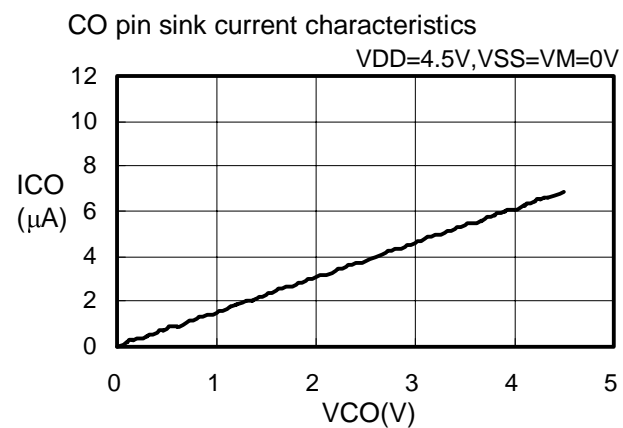
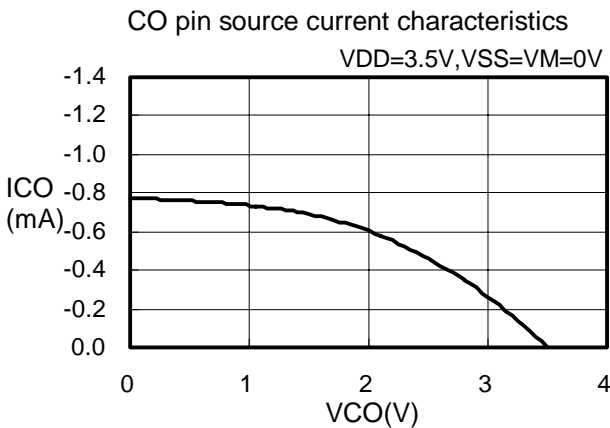




5. Delay time power-voltage characteristics (Ta=25°C)



6. CO pin/DO pin output current characteristics (Ta=25°C)

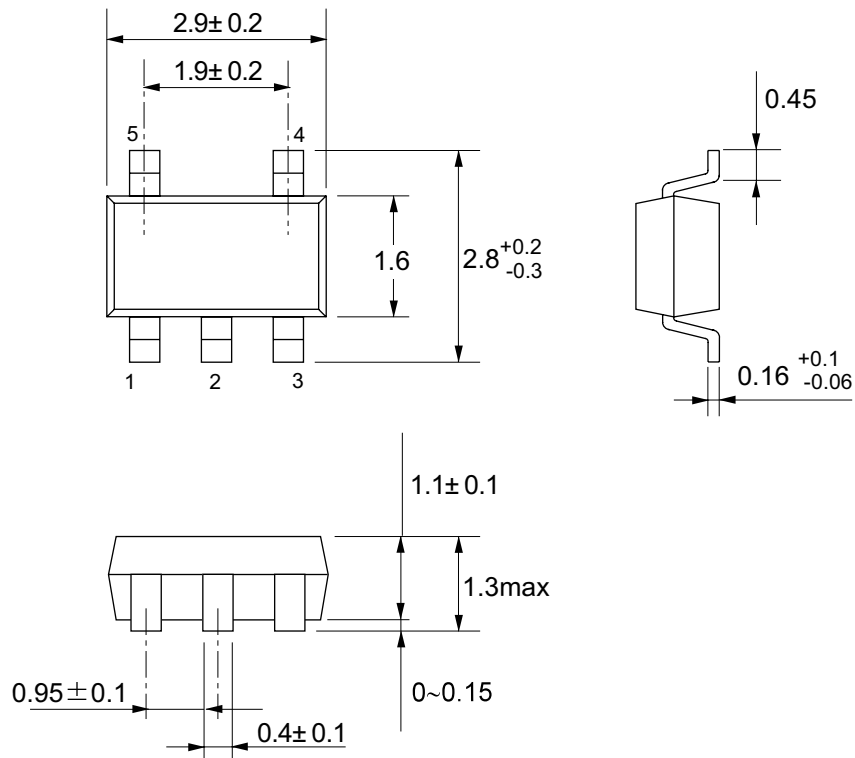


■ SOT-23-5

MP005-A 990531

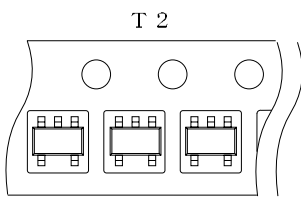
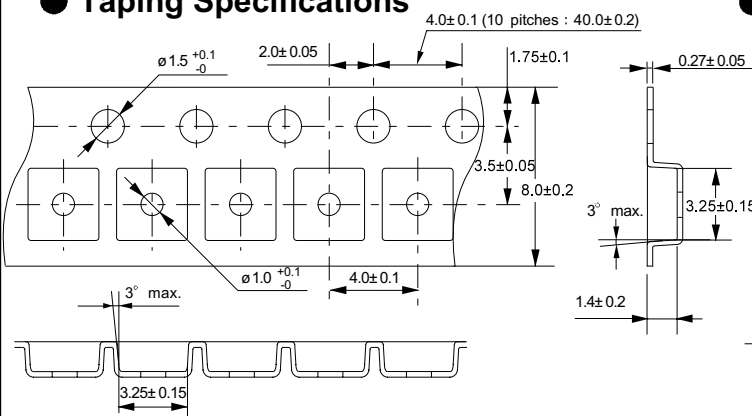
Unit : mm

● Dimensions



No. : MP005-A-P-SD-1.0

● Taping Specifications



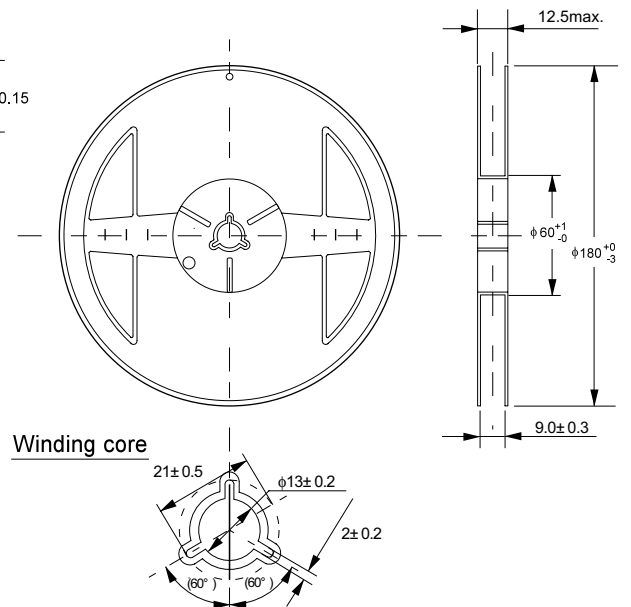
Feed direction



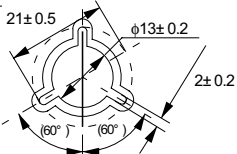
No. : MP005-A-C-SD-1.0

● Reel Specifications

1 reel holds 3000 ICs.

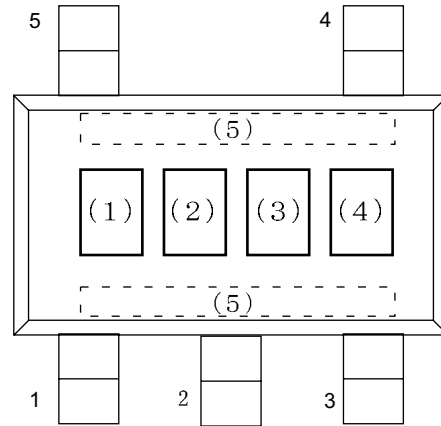


Winding core



No. : MP005-A-R-SD-1.0

● SOT-23-5



(1) to (3) : Product name (abbreviation)

(4) : Month of assembly

(5) : Dot on one side (Year and week of assembly)

No. : MP 0 0 5 - A - M - S 1 - 1 . 0

- The information herein is subject to change without notice.
- Seiko Instruments Inc. is not responsible for any problems caused by circuits or other diagrams described herein whose industrial properties, patents or other rights belong to third parties. The application circuit examples explain typical applications of the products, and do not guarantee any mass-production design.
- When the products described herein include Regulated Products subject to The Wassenaar Arrangement etc., they may not be exported without authorization from the appropriate governmental authority.
- The products described herein cannot be used as part of any device or equipment which influences the human body, such as physical exercise equipment, medical equipment, security system, gas equipment, vehicle or airplane, without prior written permission of Seiko Instruments Inc.